

# Faster discrete logarithms on FPGAs

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University of Technology

## Field Programmable Gate Arrays (FPGAs):

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- ▶ programmable *logic blocks* and a
- ▶ programmable *routing fabric*.

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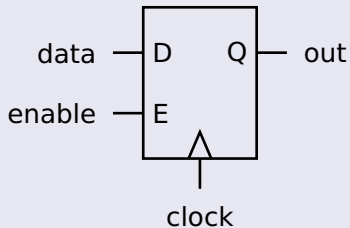
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- ▶ programmable *logic blocks* and a
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## Types of Logic Blocks:

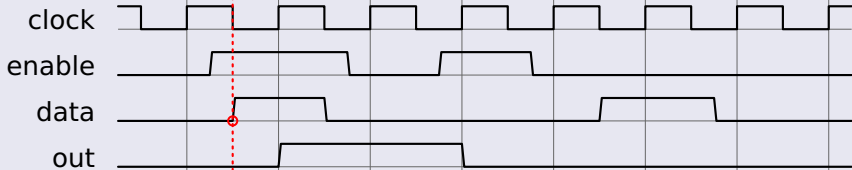
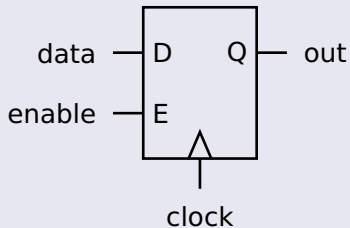
- ▶ Flip-flops (FF),
- ▶ lookup tables (LUTs),
- ▶ random access memory (block-RAM), and
- ▶ functional units: multiplier, multiplexer, memory controller, ...

## Flip-Flops: 1-bit register

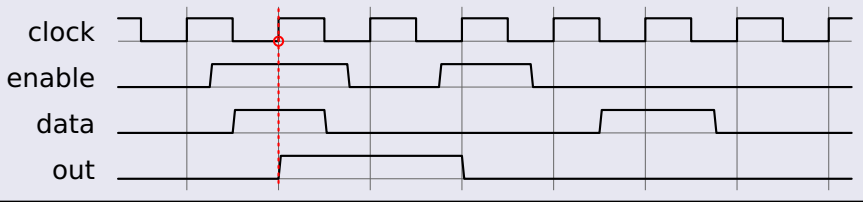
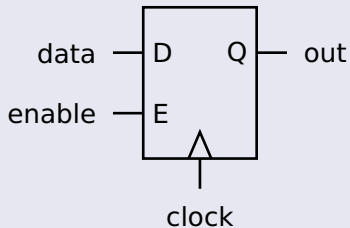




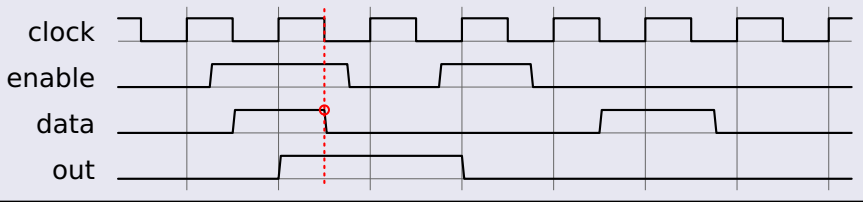
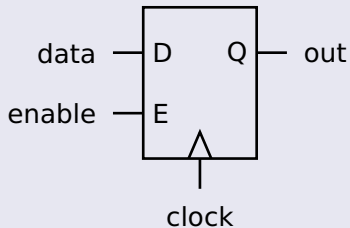
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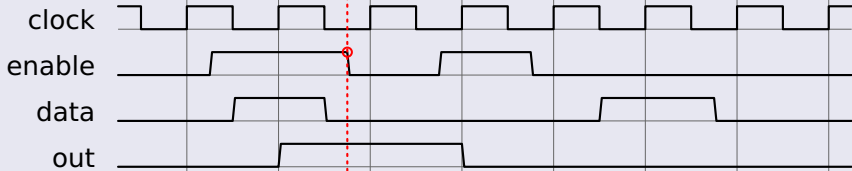
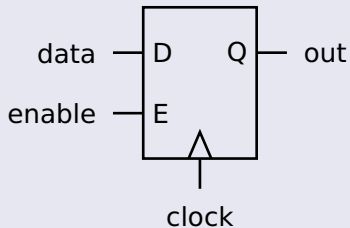


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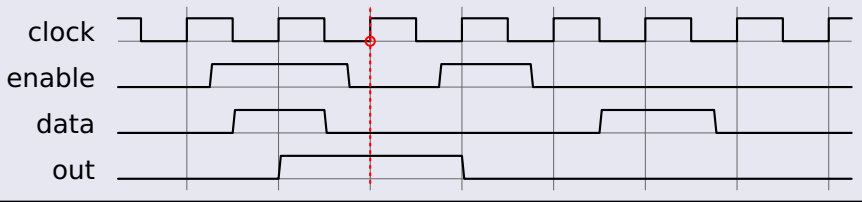
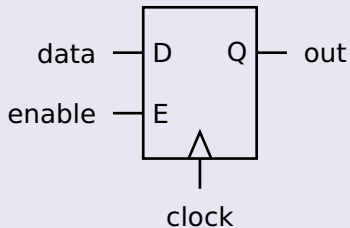




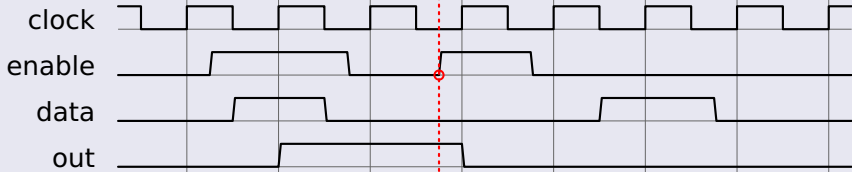
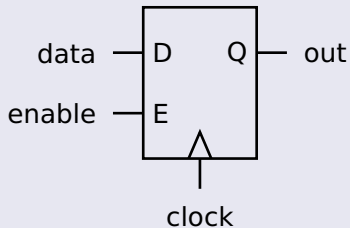
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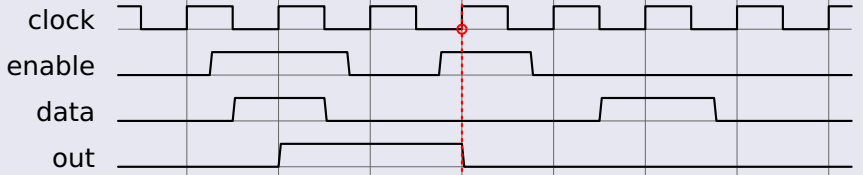
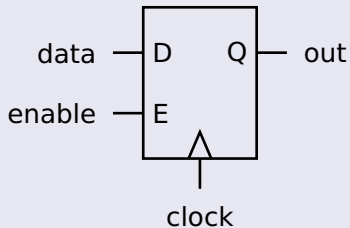
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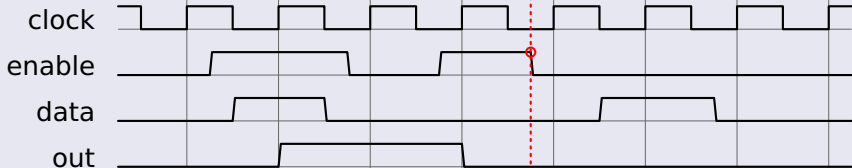
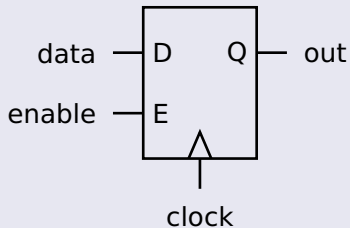
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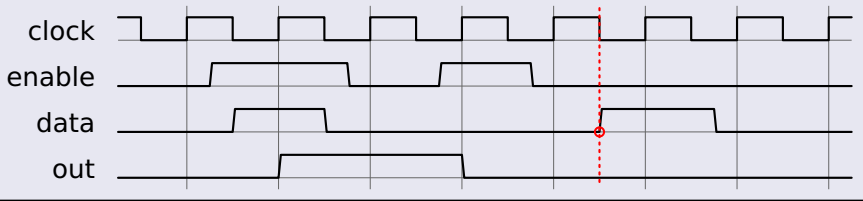
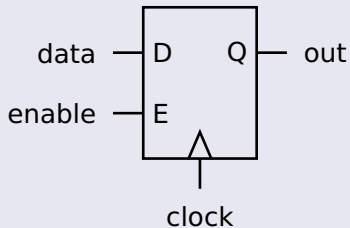
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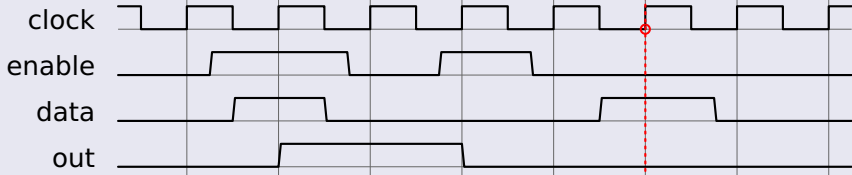
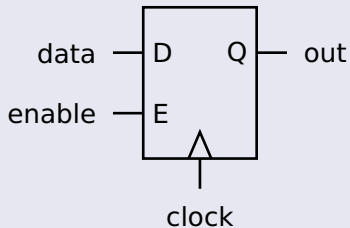
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## Lookup tables (LUTs) for implementing logic:

FPGAs use LUTs instead of logic gates, e.g.:  $x + y = z$

$x_1$	$x_0$	$y_1$	$y_0$	$z_2$	$z_1$	$z_0$
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	0	0	1
0	1	0	1	0	1	0
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0	1	1	1	1	0	0
...		...			...	



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LUT

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address	0	0	0	0	0	0	0	LUT
	1	0	0	0	1	0	1	
	2	0	0	1	0	1	0	
	3	0	0	1	1	1	1	
	4	0	1	0	0	0	1	
	5	0	1	0	1	1	0	
	6	0	1	1	0	1	1	
	7	0	1	1	1	1	0	
	...		...			...		

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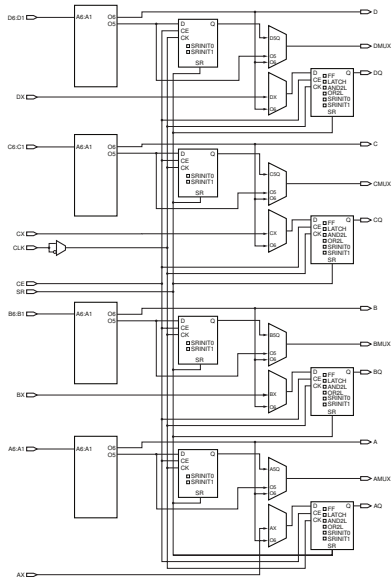
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Each LUT typically has 3, 4, 5, or 6 input lines (8, 16, 32, or 64 bit).

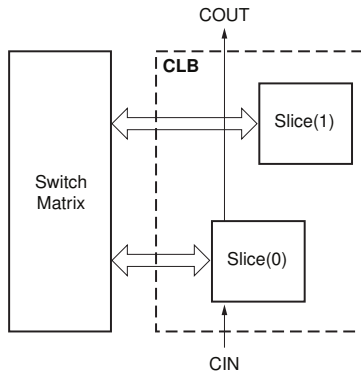
## Hierarchical Structure:

- ▶ Several LUTs and FFs form a *slice*.



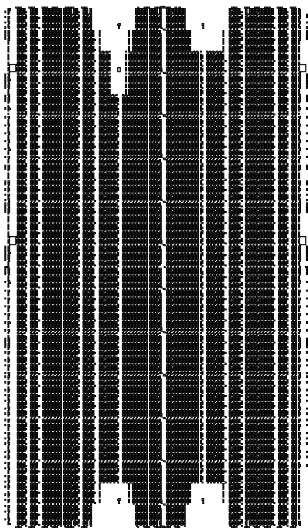
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- ▶ Several slices form a *configurable logic block* (CLB).
- ▶ CLBs, block RAM, DSP, etc. are connected by the routing fabric.



## Hardware Description Languages (HDLs)

Most common: Verilog and VHDL

High-level description language:

- ▶ Modules as building blocks,
- ▶ wires (`wire`) to connect modules,
- ▶ logic can be assigned directly to wires (synthesized as LUT),
- ▶ registers (`reg`) to store states (synthesized as flip-flop),
- ▶ clauses to define behaviour over time,
- ▶ statements for generic code creation,
- ▶ dedicated modules for specific FPGA logic blocks.



```
module poly_mult (  
    input [2:0] a,  
    input [2:0] b,  
    output [4:0] out  
);  
  
assign out[0] = (a[0] & b[0]);  
assign out[1] = (a[1] & b[0]) ^ (a[0] & b[1]);  
assign out[2] = (a[2] & b[0]) ^ (a[1] & b[1]) ^ (a[0] & b[2]);  
assign out[3] = (a[2] & b[1]) ^ (a[1] & b[2]);  
assign out[4] = (a[2] & b[2]);  
  
endmodule // poly_mult
```

$$\text{out}[2] = (\text{a}[2] \ \& \ \text{b}[0]) \ ^ \ (\text{a}[1] \ \& \ \text{b}[1]) \ ^ \ (\text{a}[0] \ \& \ \text{b}[2])$$

a[2]	a[1]	a[0]	b[2]	b[1]	b[0]	out[2]
0	0	0	0	0	0	0
0	0	0	0	0	1	0
0	0	0	0	1	0	0
0	0	0	0	1	1	0
		...				...
0	1	0	0	0	0	0
0	1	0	0	0	1	0
0	1	0	0	1	0	1
0	1	0	0	1	1	1
0	1	0	1	0	0	0
0	1	0	1	0	1	0

```
module poly_mult (input [2:0] a, input [2:0] b,
    output [4:0] out);
    ...
    LUT6 #(.INIT(64'h96665aaa3cccf000)) LUT_mul_2
    (
        .I0(b[0]),
        .I1(b[1]),
        .I2(b[2]),
        .I3(a[0]),
        .I4(a[1]),
        .I5(a[2]),
        .O(out[2])
    );
    ...
endmodule // poly_mult
```

## SECG curve sect113r2:

SECG curve sect113r2 is defined pseudo-randomly by a seed over  $\mathbb{F}_{2^{113}} \cong \mathbb{F}_2[w]/(w^{113} + w^9 + 1)$  by an equation of the form  $E : y^2 + xy = x^3 + ax^2 + b$  and base point  $P = (x_P, y_P)$ , where

$$a = 0x00006899\ 18DBEC7E\ 5A0DD6DF\ C0AA55C7,$$

$$b = 0x000095E9\ A9EC9B29\ 7BD4BF36\ E059184F,$$

$$x_P = 0x0001A57A\ 6A7B26CA\ 5EF52FCD\ B8164797, \text{ and}$$

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## Security:

The SECG standard claims 56 bits of security and comparable strength to a 512 bit RSA key.

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## Security:

The curve has been introduced to the standard in 2000 and was removed from it in 2005.

## Addition, doubling:

Addition of two points  $Q_1 = (x_1, y_1)$  and  $Q_2 = (x_2, y_2)$  on this curve produces a result  $Q_3 = (x_3, y_3)$  with

$$(x_3, y_3) = (\lambda^2 + \lambda + 1 + x_1 + x_2, \quad \lambda(x_1 + x_3) + y_1 + x_3), \text{ where}$$

$$\lambda = \begin{cases} (x_1^2 + y_1)/x_1 & \text{if } P_1 = P_2 \neq -P_2 \\ (y_1 + y_2)/(x_1 + x_2) & \text{if } P_1 \neq \pm P_2 \end{cases} .$$

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### Negative:

The negative of a point is  $-(x_1, y_1) = (x_1, y_1 + x_1)$  and  $(x_1, y_1) + (x_1, y_1 + x_1) = \infty$ .



## ECDLP:

Given a base point  $P$  and a point  $Q$ , find  $k$  such that  $Q = kP$ .

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## Naive solution:

Make an exhaustive search by checking all possible values for  $k$ .

The order of the base point  $P$  given with sect113r2 is the prime  $\ell = 5\,192\,296\,858\,534\,827\,702\,972\,497\,909\,952\,403 < 2^{112}$ .

Thus, this approach takes up to  $2^{112}$  attempts.

## ECDLP:

Given a base point  $P$  and a point  $Q$ , find  $k$  such that  $Q = kP$ .

## Better solution:

In a list of about  $\sqrt{n}$  elements from a set of  $n$  elements, there is a collision with high probability (birthday paradox).

Idea: Compute values  $R_i = a_iP + b_iQ$  with random  $a_i$  and  $b_i$ .

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$$Q = (a_j - a_i)/(b_i - b_j)P.$$

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This requires about  $\sqrt{\ell} \approx \sqrt{2^{112}} \approx 2^{56}$  points.

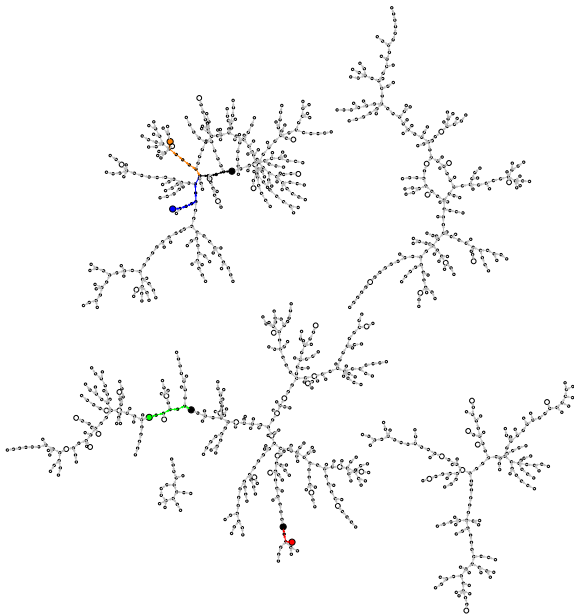
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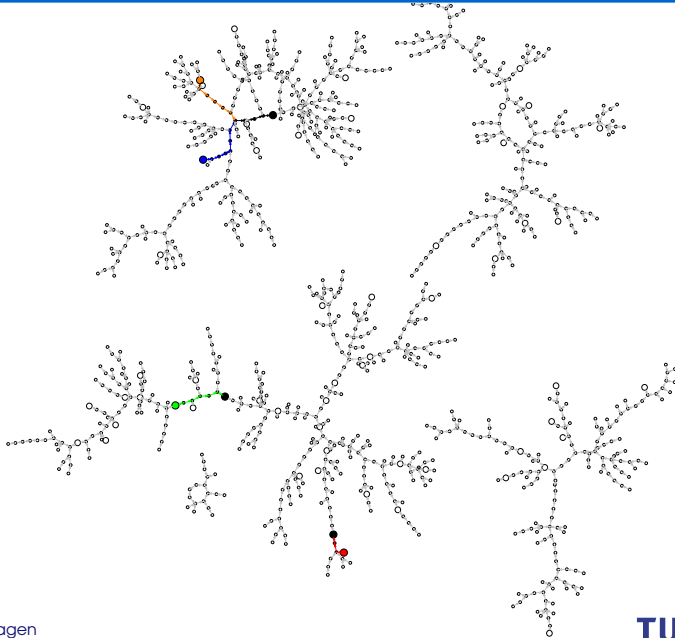
## “Best” solution:

Perform *random walks* and store only *distinguished points*.

Still requires to compute about  $2^{56}$  points  
but required storage can be reduced.

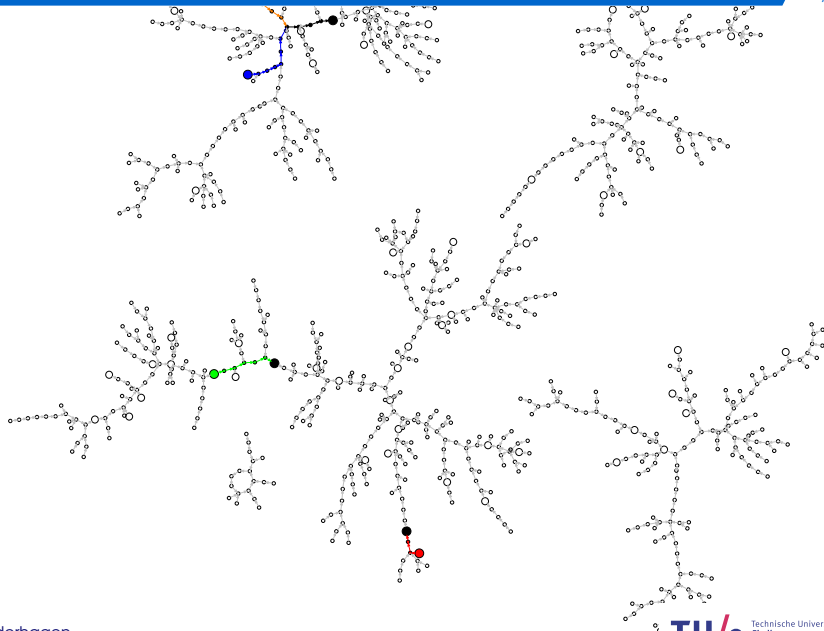






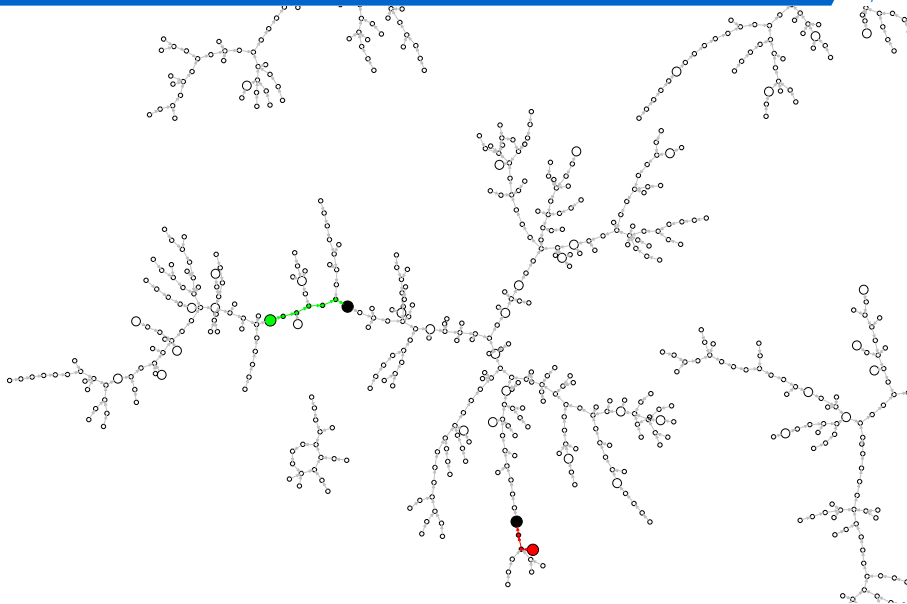
# Example: Random Walk

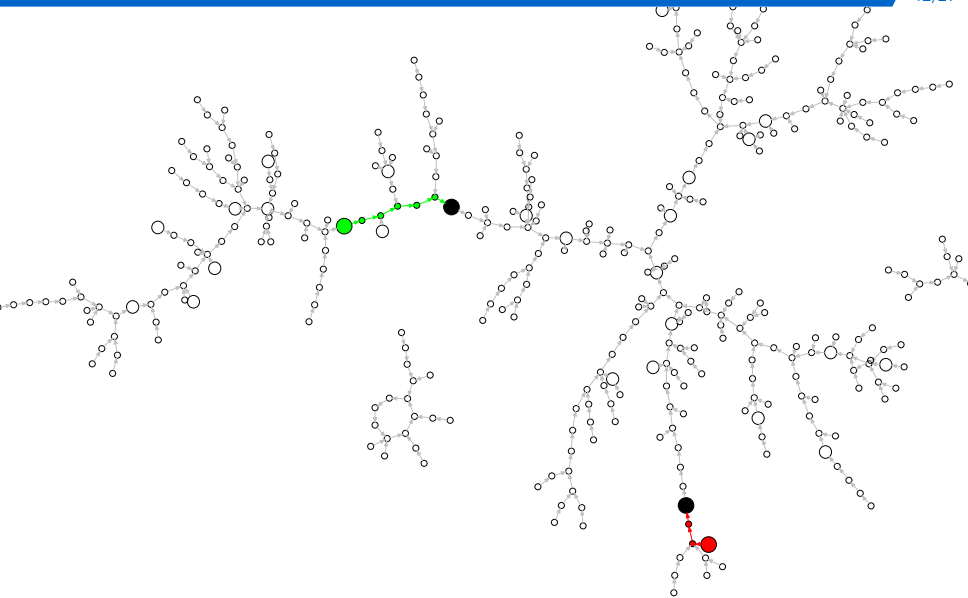
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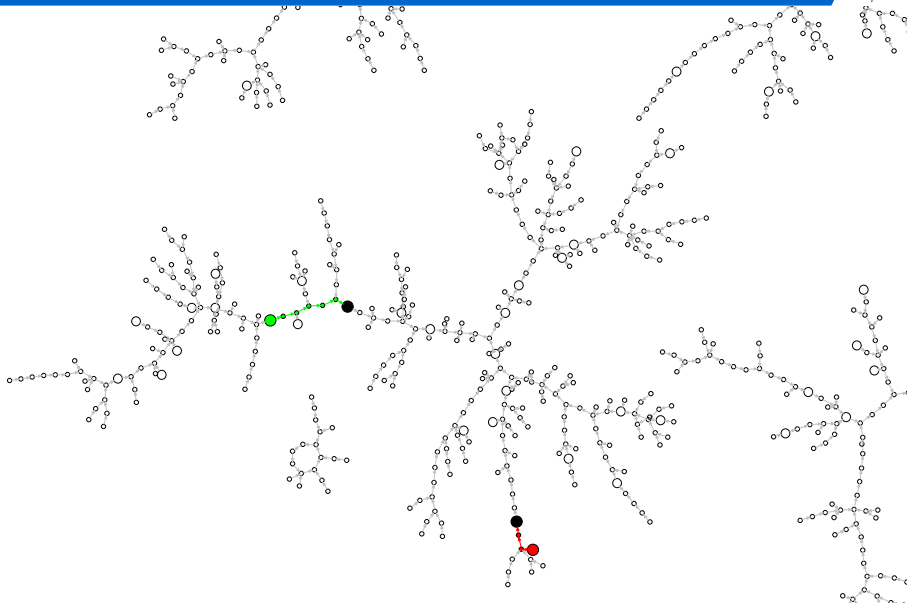
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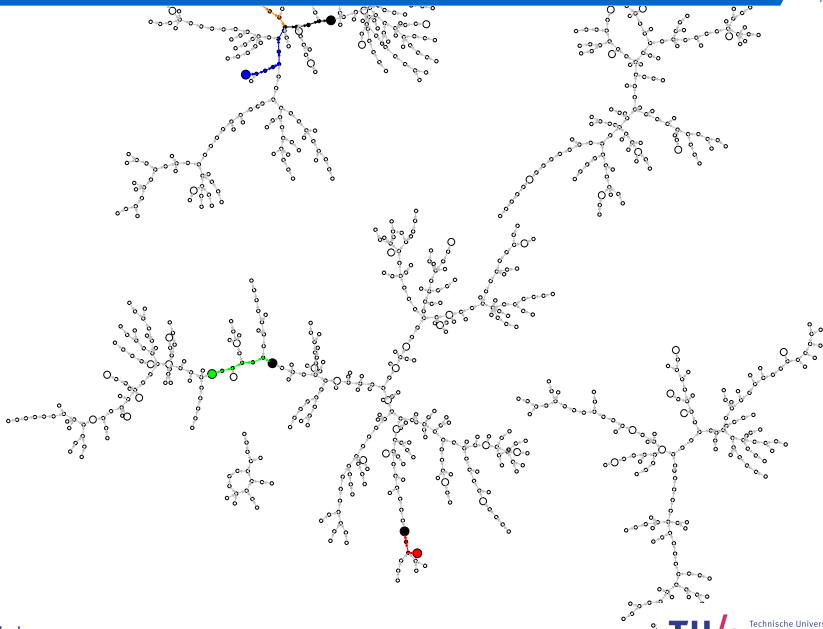
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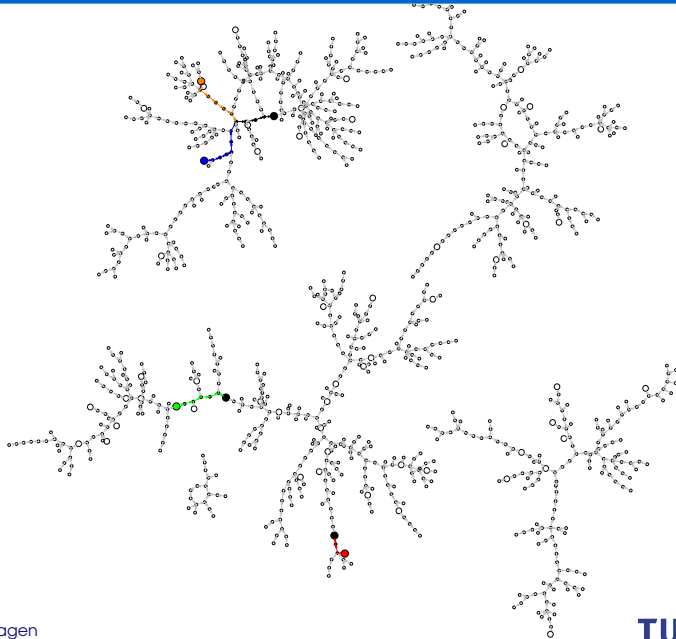
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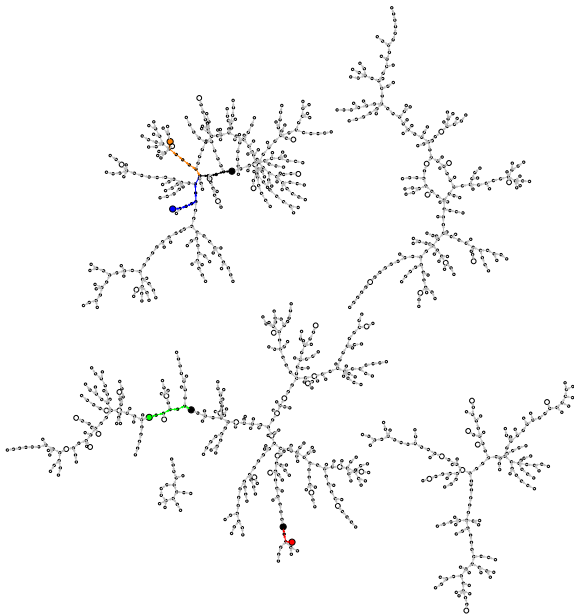


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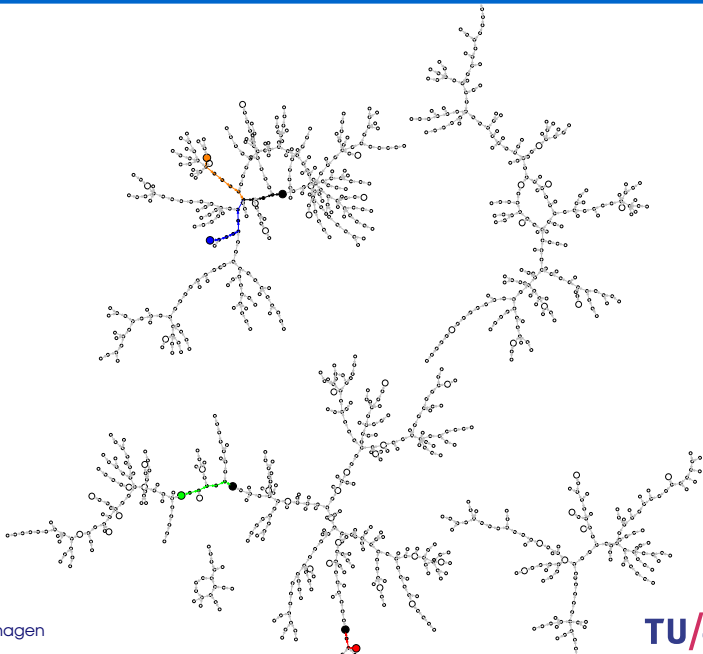
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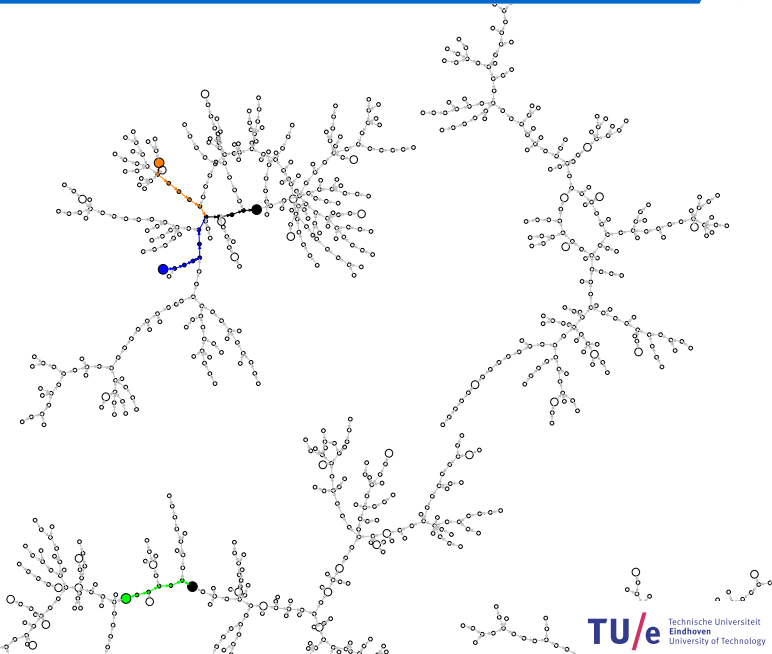


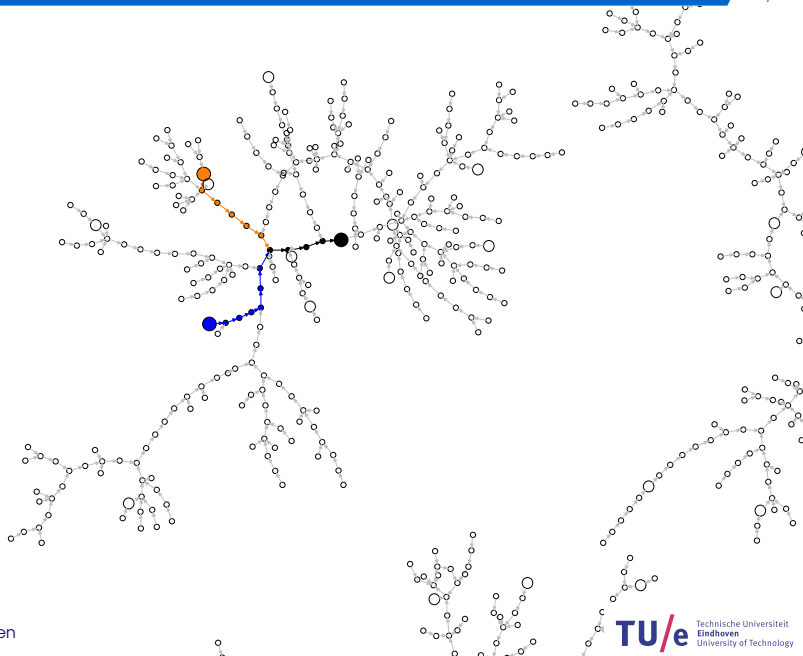


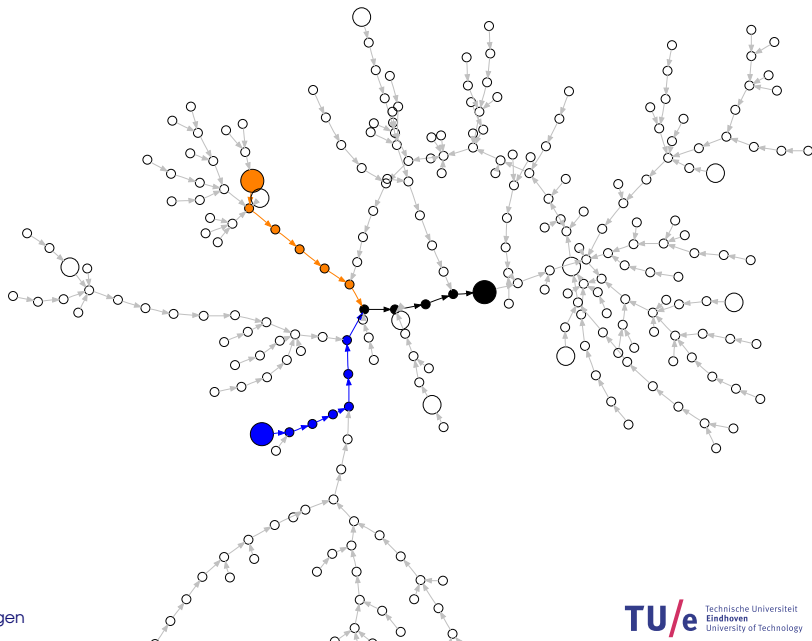












## Very suitable for parallel computation:

- ▶ Compute many independent walks in parallel.
- ▶ Distinguished points are collected by a central server.
- ▶ Once the server receives the same point a second time, derive the discrete log.

## How to perform a random walk?

Each step must depend only on the current point  $R_i$ .

Prepare a lookup table  $T = \{T_0, \dots, T_{2^t}\}$  with  $2^t$  pseudo-random points such that for each point  $T_i = a_iP$  the value of  $a_i$  is known.

Compute each starting point from a seed as  $R_0 = a_0P + b_iQ$  by deriving  $a$  and  $b$  from the seed.

For each random step, use a function

$$I : E \mapsto \{0, \dots, 2^t\}$$

(e.g., take the top  $t$  bits of the x-coordinate of  $R_i$ ) to compute

$$R_{i+1} = R_i + T_{I(R_i)}.$$

$$T_0 = t_0 P$$

$$T_1 = t_1 P$$

...

$$T_{n-1} = t_{n-1} P$$

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○  $P_i = a_i P + b_i Q$

$$x(P_i) = 01001 \dots 00001$$



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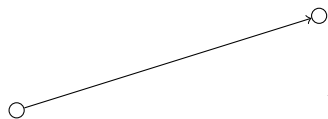
...

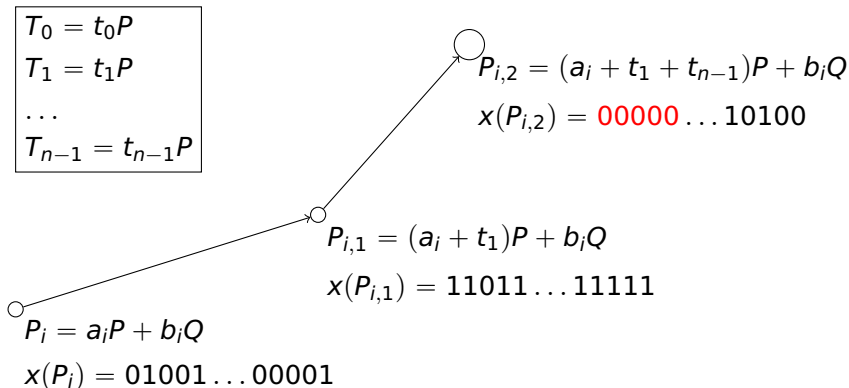
$$T_{n-1} = t_{n-1}P$$

○  $P_i = a_iP + b_iQ$

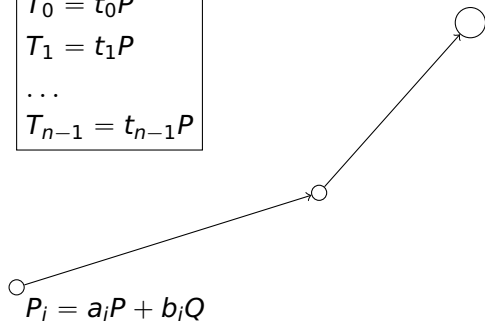
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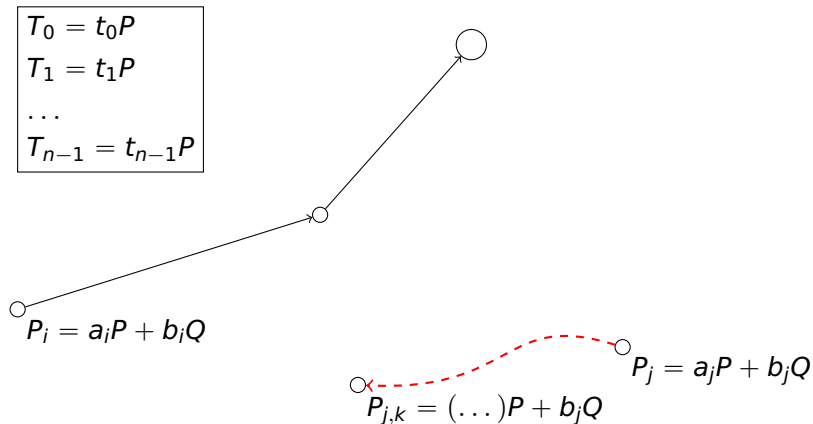

$$\begin{aligned}P_i &= a_iP + b_iQ \\x(P_i) &= 01001 \dots 00001 \\P_{i,1} &= (a_i + t_1)P + b_iQ \\x(P_{i,1}) &= 11011 \dots 11111\end{aligned}$$

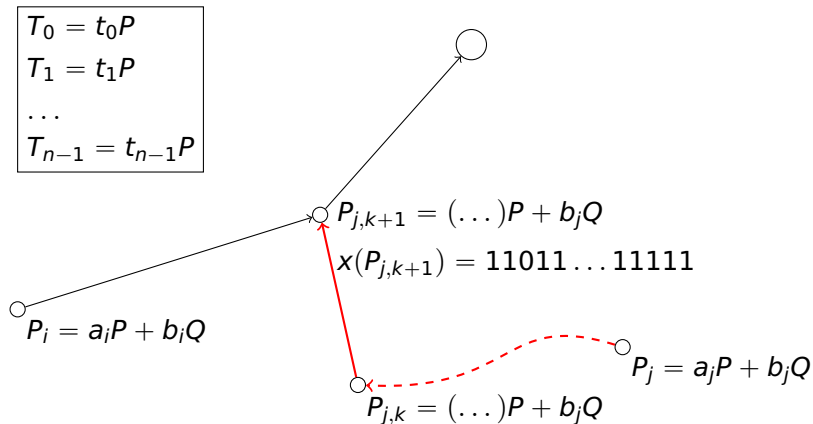


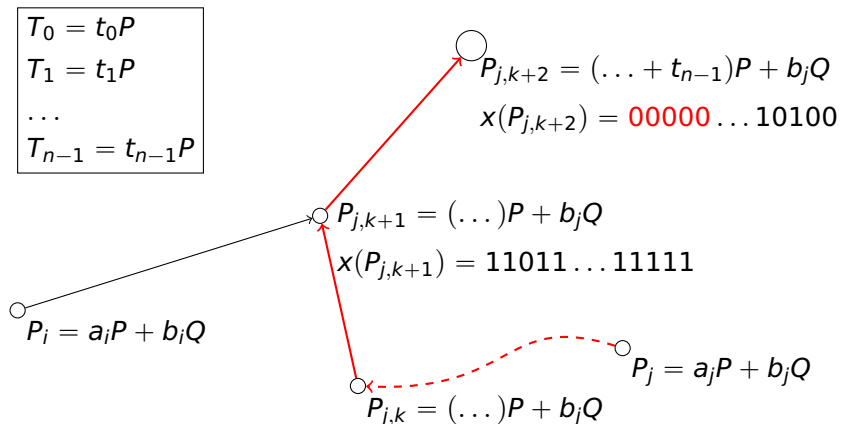
$$\begin{aligned} T_0 &= t_0 P \\ T_1 &= t_1 P \\ &\dots \\ T_{n-1} &= t_{n-1} P \end{aligned}$$



$$P_j = a_j P + b_j Q$$







## Optimization:

For each  $x$ -coordinate, there are two  $y$ -coordinates  $y_0$  and  $y_1$  giving a point on the curve:  $(x, y_0) = -(x, y_1) = -(x, x + y_0)$ .

Thus, we can halve the search space by continuing with the point  $|R_i| = (x, \min(y, x + y))$  after computing  $R_i = (x, y)$ .



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Due to the definition of the iteration function, we might encounter loops, e.g., in case  $I(R_i) = I(R_{i+1})$ :

$$R_{i+1} = |(R_i + T_{I(R_i)}i)| = -(R_i + T_{I(R_i)})$$

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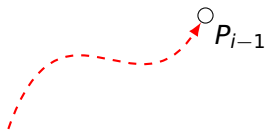
## Solution:

Detect  $c$ -cycles and leave them by computing

$$R_{i+c} = 2 \cdot \min(R_i, \dots, R_{i+c-1}).$$

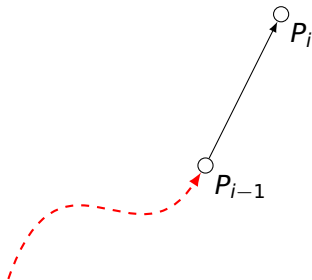
$$x_{\min} = x(P_{i-4})$$

$$\text{ctr} = 15$$



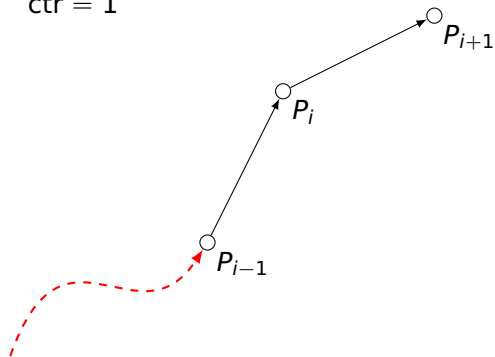
$$x_{\min} = x(P_i)$$

$$\text{ctr} = 0$$



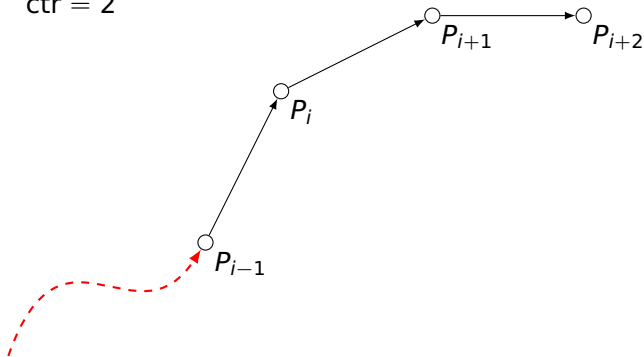
$$x_{\min} = x(P_i)$$

$$\text{ctr} = 1$$



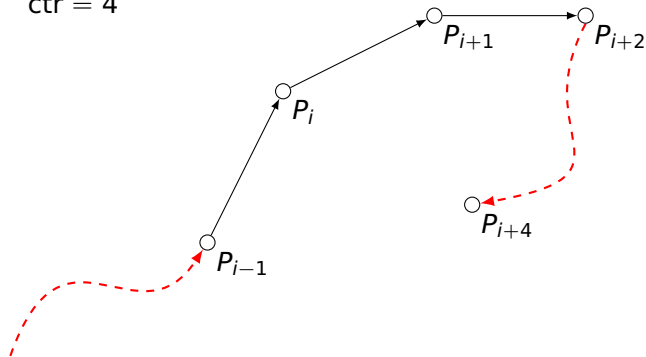
$$x_{\min} = x(P_{i+2})$$

$$\text{ctr} = 2$$



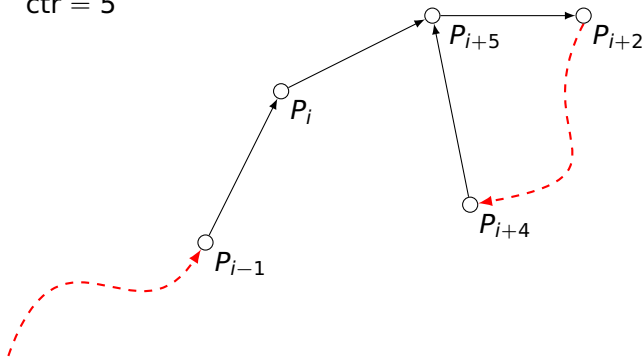
$$x_{\min} = x(P_{i+2})$$

$$\text{ctr} = 4$$



$$x_{\min} = x(P_{i+2})$$

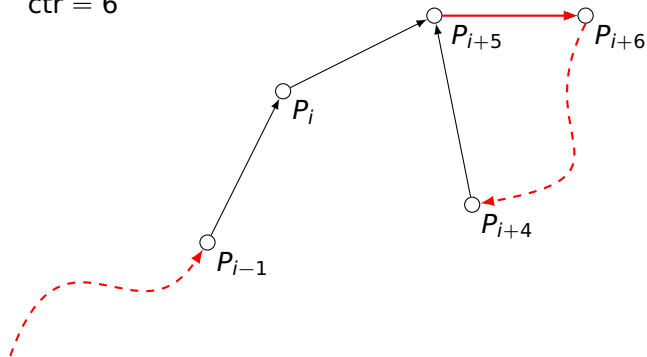
$$\text{ctr} = 5$$





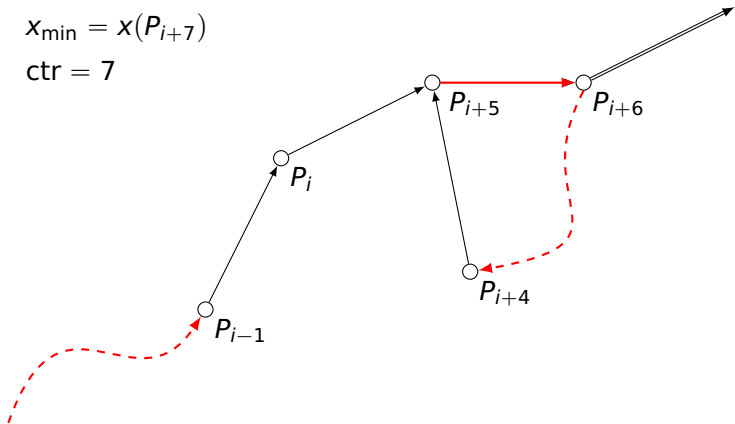
$$x_{\min} = x(P_{i+2})$$

$$\text{ctr} = 6$$



$$x_{\min} = x(P_{i+7})$$

$$\text{ctr} = 7$$



## How likely are cycles?

$n$ : entries in lookup table;  $\delta = 1/n$ .

$t$ -cycle	probability	$n = 2^{10}$
2	$\frac{1}{2}\delta$	$= 2^{-11}$
4	$\frac{1}{4}\delta^2 - \dots$	$\approx 2^{-22}$
6	$\frac{1}{2}\delta^3 - \dots$	$\approx 2^{-31}$
8	$\frac{27}{16}\delta^4 - \dots$	$\approx 2^{-39}$
10	$\frac{31}{4}\delta^5 - \dots$	$\approx 2^{-47}$
12	$\frac{1415}{32}\delta^6 - \dots$	$\approx 2^{-54}$
14	$\frac{4779}{16}\delta^7 - \dots$	$\approx 2^{-61}$

```
def random_step(x, y, seed, double, ctr, x_min):
```

```
    (P_x, P_y) = get_precomputed(x)
```

```
    x2 = x if double else P_x
```

```
    l0 = (x^2 + y) if double else (y + P_y)
```

```
    l1 = x if double else (x + P_x)
```

```
    l1 = 1/l1
```

```
    l = l0 * l1
```

```
    tmp = l^2 + l + 1 + x2
```

```
    x = x + tmp
```

```
    tmp = l * tmp
```

```
    y = tmp + y + x
```

```
    c_x_y = (x + y) < y
```

```
    y = (x + y) if c_x_y else y
```

$$(x_3, y_3) = (\lambda^2 + \lambda + 1 + x_1 + x_2, \lambda(x_1 + x_3) + y_1 + x_3), \text{ where}$$
$$\lambda = \begin{cases} (x_1^2 + y_1)/x_1 & \text{for doubling} \\ (y_1 + y_2)/(x_1 + x_2) & \text{for addition} \end{cases}$$

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```

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```
ctr = (ctr + 1) % 16  
  
c_ctr = (ctr == 0)  
  
c_lt = (x < x_min)  
  
c_new_min = c_lt or c_ctr or double  
  
double = (x == x_min)  
  
x_min = x if c_new_min else x_min  
  
ctr = 0 if c_lt else ctr  
  
return (x, y, seed, ctr, double, x_min)
```

For  $x \in \mathbb{F}_{2^{113}}$  compute  $x^{-1}$  as

$$x^{-1} = x^{2^{113}-2}$$

using an efficient addition chain.

```
def GF113_inv(din):
    r1 = din^(2^1)
    r2 = din^(2^2)
    r1 = r2 * r1
    r0 = r1^(2^2)
    r1 = r0 * r1
    r0 = r1^(2^4)
    r1 = r0 * r1
    r0 = r1^(2^8)
    r2 = r0 * r1
    r0 = r2^(2^16)
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    return r0
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## Multiplication:

- ▶ 3-level Karatsuba (and optimized LUT assignment)
- ▶ pipelined with 3-cycle latency
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## Add:

- ▶ “no” latency
- ▶ area: 60-113 LUTs (can be combined with other logic)

## Design recipes:

- ▶ ASIP: Application Specific Instruction-set Processor — “CPU” with specialized instruction set and register bank.
  - + very compact
  - large overhead
  - low latency, low throughput
  - not easy to use ALUs efficiently

## Design recipes:

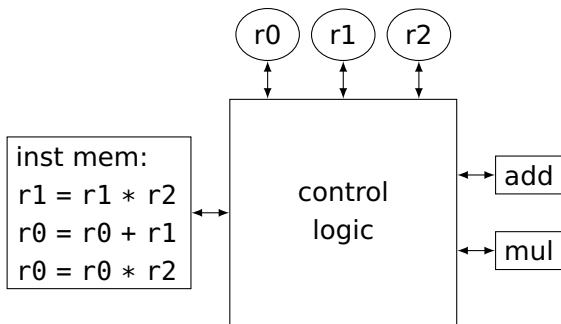
- ▶ ASIP: Application Specific Instruction-set Processor — “CPU” with specialized instruction set and register bank.
  - + very compact
  - large overhead
  - low latency, low throughput
  - not easy to use ALUs efficiently
- ▶ Unrolled: fully pipelined, one ALU per operation.
  - large area
  - + low overhead
  - high latency, high throughput
  - + relatively easy to use ALUs efficiently
  - requires many independent inputs

```
var r0, r1, r2
```

```
r1 = r1 * r2
```

```
r0 = r0 + r1
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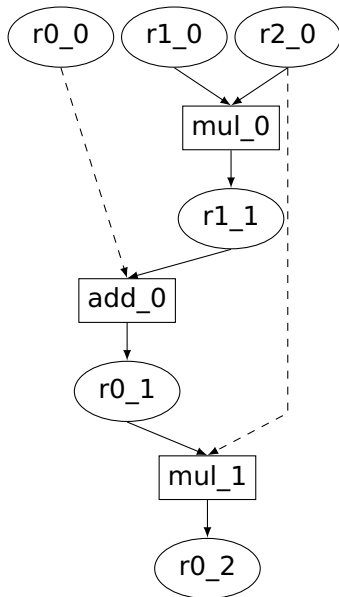


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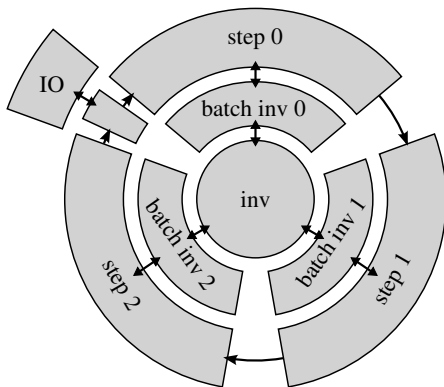


## “Hybrid” approach:

- ▶ Unrolled design for iteration function,
- ▶ ASIP design for inverter.

→ Requires Montgomery’s trick for inversion and large buffers.





## Parameters:

- ▶ 3 instances
- ▶ power consumption:
  - ▶ 8W
- ▶ area consumption:
  - ▶ 69% LUTs
  - ▶ 19% memory

---

  - ▶ 91% slices

## Runtime:

The whole computation requires about  $2^{56.3}$  iterations.

Our FPGA cluster has 120 FPGAs.

We expected the computation for a 2-core ASIP design to be finished after

$$\frac{\sqrt{\frac{\pi}{2} \cdot 2^{112} \cdot \frac{1}{2}}}{100\text{MHz}} \cdot \frac{1}{120} \cdot \frac{1}{2} \text{ seconds} \approx 31 \text{ days.}$$

Eventually, it took us about 48 days to compute the ECDLP.

## Larger DLP:

Currently we are running the attack on a generic curve over  $\mathbb{F}_{2^{127}}$  with base point of order  $2^{117.35}$ .

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- ▶ expected time to finish: last May

<http://eprint.iacr.org/2016/382>

Thank you for your attention.